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Assessment / Evaluation of the Doctoral Thesis

„Reliability Assessment and Advanced Measurements in Modern Nanoscale FPGAs"

by Petr Pfeifer

1. Topic of Research and Relevance

Reliability issues regarding nano-electronic circuits and devices have been a matter of intense research for at least the last ten 15 years. One of the major messages learnt is that nano-electronic circuits are not stable with respect to their properties and parameters, but undergo a complex aging process, which depends on electrical and thermal stress. Therefore large-scale electronic systems that consist of billions of transistors must have a built-in performance and parameter monitoring functionality in order to give reliable services over a long period of time. The question of how the essential parameters that indicate stress and aging can be monitored has been dealt with by only a few researchers, since this is a complex issue in system and circuit architecture as well as non-trivial electronic measurements. Furthermore, implementing such a complex system in an advanced IC technology is much beyond the financial limits of a normal university. The author has therefore performed basic research in this direction taking field-programmable gate arrays (FPGAs) as the physical base of his research. Even under such constraints, the research task has to be described as challenging.

2. Structure and Content of the Thesis

The thesis starts with a long and detailed table of contents. Next come list of figures, tables, abbreviations. The short preface gives the motivation for the research performed.

The first chapter starts with a short introduction of FPGAs. The author might have added that FPGAs are different in structure from standard CMOS logic, but modern FPGAs, beyond programmable logic blocks, often contain arithmetic units in standard CMOS or even processor-cores in standard logic design. The author then gives an overview over known mechanisms of aging, parameter shifts and causes of permanent damage. Sub-chapter 1.1 starts with a short history of semiconductor technology and then shows the importance of semiconductor reliability, FPGA reliability and aging effects by measuring the number of publications over time. Here the author develops the central argument of his thesis that embedded RAM-blocks (BRAM) of FPGAs may serve as the essential instrument for supervision and monitoring. This is the starting point for the innovative concept of a "reliability lab on chip", which makes the core of this thesis. Figure 4 gives an overview over technology development for on-chip parameter measurement, starting with direct transistor contact measurements and ending with an on-chip computer core that governs a built-in self test of crucial parameters. Sub-chapter 1.2 only presents the structure of the thesis, 1.3 highlights the problems to be solved, and 1.4 gives a summary of the essential contributions.

Chapter 2 describes the "state of the art" and presents a theoretical framework. Theory starts with well-known considerations on reliability and dependability, including the bath-tub curve. 2.3 introduces existing standards for reliability measurements and prediction. From 2.5 has an emphasis is on CMOS technology and specific fault effects. The author describes