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Assessment / Evaluation of the Doctoral Thesis

„Reliability Assessment and Advanced Measurements in Modern Nanoscale FPGAs"

by Petr Pfeifer

1. Topic of Research and Relevance

Reliability issues regarding nano-electronic circuits and devices have been a matter of intense research for at least the last ten 15 years. One of the major messages learnt is that nano-electronic circuits are not stable with respect to their properties and parameters, but undergo a complex aging process, which depends on electrical and thermal stress. Therefore large-scale electronic systems that consist of billions of transistors must have a built-in performance and parameter monitoring functionality in order to give reliable services over a long period of time. The question of how the essential parameters that indicate stress and aging can be monitored has been dealt with by only a few researchers, since this is a complex issue in system and circuit architecture as well as non-trivial electronic measurements. Furthermore, implementing such a complex system in an advanced IC technology is much beyond the financial limits of a normal university. The author has therefore performed basic research in this direction taking field-programmable gate arrays (FPGAs) as the physical base of his research. Even under such constraints, the research task has to be described as challenging.

2. Structure and Content of the Thesis

The thesis starts with a long and detailed table of contents. Next come list of figures, tables, abbreviations. The short preface gives the motivation for the research performed.

The first chapter starts with a short introduction of FPGAs. The author might have added that FPGAs are different in structure from standard CMOS logic, but modern FPGAs, beyond programmable logic blocks, often contain arithmetic units in standard CMOS or even processor-cores in standard logic design. The author then gives an overview over known mechanisms of aging, parameter shifts and causes of permanent damage. Sub-chapter 1.1 starts with a short history of semiconductor technology and then shows the importance of semiconductor reliability, FPGA reliability and aging effects by measuring the number of publications over time. Here the author develops the central argument of his thesis that embedded RAM-blocks (BRAM) of FPGAs may serve as the essential instrument for supervision and monitoring. This is the starting point for the innovative concept of a "reliability lab on chip", which makes the core of this thesis. Figure 4 gives an overview over technology development for on-chip parameter measurement, starting with direct transistor contact measurements and ending with an on-chip computer core that governs a built-in self test of crucial parameters. Sub-chapter 1.2 only presents the structure of the thesis, 1.3 highlights the problems to be solved, and 1.4 gives a summary of the essential contributions.

Chapter 2 describes the "state of the art" and presents a theoretical framework. Theory starts with well-known considerations on reliability and dependability, including the bath-tub curve. 2.3 introduces existing standards for reliability measurements and prediction. From 2.5 has an emphasis is on CMOS technology and specific fault effects. The author describes

all relevant fault effects that are related to aging. NBTI versus PBTI (negative / positive bias thermal instability affecting PMOS/NMOS transistors) is discussed presently, NBTI is the dominating effect, PBTI has also been observed with about only 20% of the NBTI-induced effects on transistor delays. In section 2.6 electro-migration as one 4main reason for aging is discussed, followed by NBTI in 2.7. Section 2.8 refers to single-event transients and single-event upsets, which perform a class of fault effects which is independent from aging and parameter deterioration. The author considers these fault effects, which affect storage elements in particular, as "covered" by the memory implementation in his target system. 2.9 gives a short introduction to testing and testability issues showing various classes of faults. Here it cannot be concluded how aging-relevant parameters will be measured. Beyond hard-type faults and soft-type faults mentioned, intermittent faults play a significant role in real circuits.
Section 2.10 deals with methods of testing devices under various environmental conditions, whereby overvoltage, temperature and humidity play a significant role. The list does not include tests under conditions that are mainly important for transient and intermittent faults such as:

- VDD / GND noise
- Electromagnetic radiation
- Particle radiation.

This limitation is acceptable, since the author has a focus on wear-out and aging effects.
Sections 2.11 and 2.12 deal with the general structure of FPGAs first and then with FPGA-specific reliability issues. Reliability of FPGA structures has recently become an important issue, since FPGAs are not only used for rapid prototyping and design validation. They also play an important role in target systems, where specific circuits are needed in small production volume, such as satellites and space applications. As the physics of FPGA-logic is based on SRAM-like memory cells, they will show a fault behavior which is not identical with CMOS logic of the same fabrication technology. 2.13 discusses aging and variability in parameters. Section 2.14 finally has a focus on critical paths. Here it is not mentioned that critical paths on FPGAs, where interconnects are programmable, may differ significantly from critical paths in normal CMOS logic.

The third chapter is entitled "description of the new method", possible meaning the new method of supervising aging-relevant parameters. The method starts from the assumption that aging effects can at best and in general be monitored by measuring delays. This is one real possibility, but, for example, measuring currents and temperatures may also be useful. Signals are sampled at different rates in order to extract the necessary information, and results are stored in the BRAM cells. The design of the test oscillator is discussed in section 3.2. Ring oscillators including all relevant devices are used as the essential monitoring elements that may show parameter shifts. Note that in FPGAs, unlike standard logic, certain devices and building blocks may either be used as monitoring elements or, after re-synthesis under suitable constraints, in functional units. The technique of how to build such an oscillator including the right elements is then a critical problem.
Section 3.3 describes the use of BRAM-blocks on FPGAs for the storage of measured data, but the BRAMs also incorporate sampling units necessary for data acquisition. The structure of BRAM block, their access mode, size, and locations on FPGAs are shown in detail. Section 3.4 discusses the problem of signal sampling with a specific focus on under-sampling (with sampling frequency below the double of the maximum signal frequency). Apparently, as explained in 3.5, 3.6 and 3.7, under-sampling is suitable for specific types of

measurements. Measurements, as discussed in section 3.8, can be done based on absolute or on differential values, which yield more information in case of e. g. stress-related parameter shifts. Sections 3.9 and 3.10 discuss sensitivity and resolution for different types of FPGAs and oscillator start-up and noise, respectively.

The 4th chapter describes experiments and results. The author uses FPGAs of different types and generations with a minimum feature size from 65, 45 and 40 nm down to 28 nm. From 4.2 the author describes his own software tools used to perform the test routines. For the measurement of FPGA voltages and for voltage adjustments, in some cases external potentiometers were added to the boards. Measurements of local temperatures on FPGAs are essential for stress analysis, but they are also difficult in terms of test access and parameter extraction. The extra equipment used for this purpose is a thermos-electric element in combination with a controllable fan as cooling device. Unlike (much more expensive) temperature chambers such a set-up limits the environmental temperature; excluding the temperature range much below 0 C. Section 4.6 contains selected results. Measurements are typically performed at variations in temperature and in supply voltage. Interactions by electrical orc thermal coupling between different oscillator rings are also analyzed.

With voltages varied between about 0.6 V and 1.5 V (45nm SPARTAN) and between 0.9 V and 1.2 V (28 nm Zynq) oscillator show a shorter duty cycle for higher voltages. Remarkably, the 28 nm te3chnology has a smaller active voltage range than the 45 nm version, specifically with respect to low voltages. Furthermore, the 28 nm technology seems to be more power hungry.

The next series of measurements aims at measuring performance degradation and aging. For this purpose, devices were operated under different temperatures of the package between 0 C and 130 C. Oscillators show a regular behavior at temperatures up to 90 C, which is quite a remarkable value, both for 28 and for 45 nm structures. For devices in 65 nm and 45nm technologies, investigations are performed which show a clear picture of negative / positive bias thermal instability affecting the duty cycle of a normally balanced clock signal. The test results for 28 nm technology are less clear.

Further measurements clearly exhibit a direct relation between supply voltage and core power dissipation / temperature. The section named “conclusions” explains that 45 nm technology FPGAs are superior in terms of power dissipation, but the 28 nm technology allows for a combination of two CPU cores with a programmable section of about equal size. Unfortunately, the author has not been able to analyze the aging behavior of sub-circuits and devices in the processor cores.

The 6th chapter deals with the detection of aging-induced delay faults. While specific circuitry for the detection of delay faults on critical paths is a hot research issue for CMOS logic, there is little work known on this problem in FPGAs. The solution proposed by the author is to use the timing features of the BRAM block and sample a signal twice in successive clock periods. The “fast path” problem encountered in normal logic is not mentioned, but may exist. The implementation is described in detail, and in section 5.4 results are presented. This way the author has devised an “XOR-less" aging detector, specifically useful for advanced FPGAs.

Chapter 6 deals with the integration of previously described partial solutions into large-scale systems. This includes a proper segmentation of the available memory. Then the process of preparing an FPGA for on-chip monitoring is outlined. This includes system partitioning for interchange of active and tested parts. Sub-sections 6.6 to 6.8 describe a scaling experiment done with implementing a VLIW processor core a various FPGA platforms.

The 7th chapter entitled “conclusions” includes a sum-up of contributions, a critical assessment of the work done, and recommendations for future work.

The rest of the thesis consists of a list of a comprehensive bibliography, a list of publications, a glossary, and an index list.

3. Summary

The candidate has given a substantial contribution to the “state of the art” in an area, which is badly needed for dependable systems, but receives too little attention elsewhere. The author has developed a systematic approach towards an innovative measurement strategy for aging

effects on FPGAs, which is innovative and of real practical importance. It should have a real impact on the systematic construction of long-term dependable FPGA-based systems. The thesis is very comprehensive and goes into the essential details. It is well written and contains enough and high-quality pictures and graphs. With respect to length and contents it is well beyond the average of doctoral theses in this field of research. The list of publications (50!) is impressive. The candidate has already earned himself a reputation as an expert for FPGAs and related wear-out / aging effects at an international level. Compared with other theses, the work presented is well above average and truly "outstanding".
Therefore it is proposed to continue the graduation process. The work is recommended for defense.

Cottbus, Jan. 21st, 2015

Prof. Dr. H. T. Vierhaus

Questions:

1. Which parts of the work are specific to FPGAs and which can be used for CMOS logic?
2. How do you treat embedded CMOS blocks (ALUs, multipliers etc.) on FPGAs?
3. How can you deal with embedded processor?
4. Can the methods be expanded to observe parameter shifts in analog circuits?
5. Is there a way to observe aging effects beyond delays, e. g. by current measurements?

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Statement of the evaluation of the doctoral thesis

„Reliability Assessment and Advanced Measurements in Modern Nanoscale FPGAs"

by Petr Pfeifer

Scientific significance

The development of new technologies in design and manufacturing of advanced integrated circuits allows higher integration of complex structures at ultra-high nano-scale densities. The continuous advancement in manufacturing yield and field reliability are important enabling factors for electronic systems which are pervading nearly all fields of our life. On the other hand, the electronic circuits of new generation are becoming more and more sensitive to different negative effects of various changes of internal nanostructures and parameters. Changes in parameters due to process variations and aging along the working lifetime, as well as power supply voltage and temperature variations, can result in significant signal delays which in their turn may affect the final design quality and dependability. Such critical changes have to be detected before they may result in system failures.

For this reason, the extremely fast downscaling of semiconductor technology makes reliability the main concern in future design and development of new microelectronics and nanotechnologies.

The main target of this thesis is to develop a new reliability methodology which opens a novel precise way of in-situ measurement of parameters in devices and circuits, reliability testing, and better estimation of reliability parameters with their periodic assessments. The importance of the research topics covered in the thesis is very high, and the advancements of the current state-of-the-art in the reliability measurement and assessment of electronic devices and systems achieved by the candidate are scientifically and practically extremely significant.

Contribution of the work

The main contributions of the thesis can be listed as follows:

- A new reliability methodology and also its key theory background was developed with opening new ways for easy and precise in-situ measurement of reliability parameters and parameter shifts in electronic devices and circuits.
- A novel low-cost and reconfigurable lab-on-chip concept of on-chip test generation and analysis based on using Block RAM data streams and signal sampling with focusing on undersampling was developed. The new methods do not need expensive external measurement equipment. They are directly linked to quality issues of devices, allowing a wide range of parameter measurements, delay testing, and aging assessment fully on-chip.

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- The developed new approach includes multi-platform solutions, new equations, XOR-less aging detection unit and also the key differential aging measurement mode using Block RAMs.
- A lot of new data and results from measurements and experiments on various technologies down to very popular 28 nm were presented, analysed and discussed.

The main content of the work

Chapter 1 gives a short overview about the background, motivation, problem statement, and contributions of the work.

Chapter 2 presents state-of-the-art, and gives an overview about the theoretical grounds of the research field. A large set of topics related to the dependability research, reliability parameters and assessment, reliability prediction methods, CMOS design, electromigration, bias temperature instability, single-event transients and upsets, testing and testability issues in general, an overview about FPGA technology reliability as well as aging and parameter variability issues. The Chapter ends with redefinition of the traditional term of critical paths as aging-critical paths.

The main theoretical results are presented in Chapter 3 where the description of the new method developed by the applicant is given in details. First, the new method is described in general. Then the basic principle of on-chip parameter measurement using the differential method is discussed. Chapter 3.2 is devoted to the design of test oscillators, and thereafter in Chapter 3.3 the description of the novel idea of utilization of Block RAMs is presented, and its advantages are discussed. The presented approach is new in its background as well as application. In Chapters 3.4 - 3.7 the idea and use of undersampling for measuring the frequency are thoroughly discussed. In Chapter 3.8 the two key methods called absolute and differential are compared. Both of them can be implemented under the proposed methodology whereas the propsed in the thesis differential method is a completely new method invented by the candidate. Chapter 3 ends with discussion of the method's sensitivity and resolution aspects.

Chapter 4 presents experimental results. The author has contributed with a huge amount of experimental research, testing the validity of his hypotheses with close to hundred different tests on many platforms. The results of his experimental research fully validate the new proposed methodology and demonstrate its desired quality. The values obtained are important for proper simulations and modelling of the design parameters in FPGAs, and as well in other VLSI circuits.

Chapter 5 presents a completely new solution as a new way of utilization of Block RAM for the delay fault detection purposes. The presented solution has advantages, like easy implementation in the existing designs, where a CPU core is available. The candidate indicates as well on the disadvantages of the approach regarding the increase of power consumption, and regarding the lower ability to detect delays on short paths.

Chapter 6 deals with implementation of the methodology and the solutions developed in the thesis in various complex systems. The chapter demonstrates a wide scope of international cooperation where the applicant has been involved.

Chapter 7 concludes the thesis and highlights the most important contributions of the candidate.

Conclusions and discussion

The candidate has demonstrated excellent argumentation and maturity in discussions, and was able to present a clear synthesis of the current state of the research and new knowledge, indicating as well new paths for further research. In some cases, however, the own contributions of the candidate were not sufficiently compared with currently available or previously used similar solutions or methods.

Composition and presentation

The presented doctoral dissertation is an impressive scientific work and is well approved through the very long list of publications and presentations of the candidate. The thesis has a clear structure and presents well the contributions of the candidate.

Remarks and questions to the thesis

1. In Chapter 3, a new differential method is proposed. What are the main advantages of the new method and implementation compared to the previous solutions referenced as [68] and [69]?
2. The Sub-Chapter 3.10 discusses the ring-oscillator theory. The candidate compares his own results regarding the exact case with other methods, and he claims that „it is obvious" that his approach outperforms the other methods. Which arguments allow to make this conclusion?
3. Chapter 4 ends with a statement that the results obtained can be used not only for FPGAs, but as well for other VLSI products. Can you justify this claim in more details.
4. Why are you saying that the inability to detect small delays is a disadvantage of the new delay detection method developed in the thesis (Chapter 5)? The more suitable criterion could be „detection of delays that may cause errors in the functioning of the circuit". Can you comment this point?

Conclusions:

The presented doctoral work is impressive, has clear contributions to the scientific community, and is sufficiently approved by publications in internationally recognized journals and conferences.

Mr. Petr Pfeifer has demonstrated in his dissertation his ability of independent creative work in the field of Integrated Circuits Reliability. His work meets the required standards of the doctoral thesis and I recommend this work for defense.

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Tallinn, January 18, 2015

Review of Doctoral Thesis: "Reliability Assessment and Advanced Measurements in Modern Nanoscale FPGAs"

Thesis author: Ing. Petr Pfeifer

The submitted doctoral thesis deals with methods for evaluation of reliability of digital circuits based on modern semiconductor structures. The speed of technology innovation is very high in the semiconductor industry as well as the utilization of modern technologies in safety critical applications. From this perspective, reliability of integrated circuits belongs to main concerns in design and manufacture.

The thesis consists of seven chapters. Chapter 1 states the background and motivation. Chapter 2 describes main phenomena which can lead to the circuit malfunction. The existing test methods are also very briefly described there. My comments follow:

- Chapter 2 does not include description of existing methods which could be used as a reference in the experiments. There is also missing a conclusion which clearly defines the advantages and disadvantages of existing methods. The author shall define the thesis objectives based on that.
- Important terms are described without any reference (e.g. NBTI, HCI pg. 28).
- The test methods are described very briefly without any reference (Section 2.10, pg 38). It is not possible to distinguish between production and qualification tests.

Chapter 3 exhaustively describes a new method which shall recognize degradation of CMOS structures caused by NBTI or PBTI. I consider this approach as innovative and easily implementable in FPGA.

Chapter 4 describes experiments used to asses performance of new method. My comments follow:

- Comparison with existing approaches is missing. Indeed, it can be difficult to find prior publication on the same topic. However the author could compare the performance of method with approaches for the measurement of frequency or duty-cycle.
- Absolute values should be used instead of undefined relative variables in figures 42, 43.
- Figure 45 is redundant. All data is presented in figure 44.
- The description of y-axis in figure 46 is confusing (100% does not equal to 1.0V).

Chapter 5 is dedicated to the description of delay-fault detector based on BRAM. I consider this part redundant in the thesis because it does not comply with the main theme.

Implementation aspects of developed method are discussed in chapter 6. From my perspective, this part of thesis is too general. More specific recommendations shall be provided before the proposed method can be implemented to real test methodology.

Chapter 7 provides a summary of presented work and point topics for future research.

Questions for defense of a thesis:

- Can you compare features of presented method with approaches published in [13], [14], [15], [16]?
- How is independence of oscillators managed? Does the interference limit the number of oscillators running in a single FPGA?

Summary – I appreciate that Mr. Pfeifer has chosen for his research really actual topic which can be very interesting also for industry. The presented method demonstrates nice utilization of well-know under-sampling technique. I admire amount of effort put into experiments. I would expect better presentation of experiments as well as evaluation and comparison of results. The list of publications proves author's ability to come up with original results.

Despite the comments mentioned above, I support Mr. Pfeifer's candidacy to receive PhD degree. I recommend this thesis for defense.

In Brno, Jan 27th, 2015

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